

# Revolutionary Improvement to Existing CPU Performance Possible via Novel Approach Featuring Multiple Processor Clocks Embedded in Processor Pins Routing Discrete Computational Requests Through Shared Physical Architecture

22 June 2023

Simon Edwards

Research Acceleration Initiative

## Introduction

In light of much stagnation over the past 15 years in the field of microprocessing, the community stands divided between those focused on the miniaturization of transistors and those hoping for a revolution in the area of quantum computing; an area that, in fact, encompasses a wide variety of experimental avenues which, at best, will merely augment existing architectures i.e. they are useful for handling large prime numbers, not for high-throughput operations. When Phononic Collision Matrix processors, for instance, become publicly available, they will be featured as mere sub-modules of commercial CPUs (similar to integrated graphics modules.) Regrettably, there is likely to be substantial resistance to the commercial release of that technology (and likely the one about to be described, as well) given its ability to “break” existing public key encryption schemes.

Virtually none are working to identify areas in which underlying assumptions regarding the limits of traditional microprocessors are holding back their true potential. Alas, many of the commercial gimmicks of the last decade and a half have only served to cripple performance sc. Multi-core and multi-thread processing.

In this publication, I will explain how a technique already in use in other fields such as cellular communication may be applied in a revolutionary way in order to produce a 200-300 fold improvement to flops-per-second performance of existing architectures by modifying the architecture of processor pins and by beefing up the pipeline bandwidth between the RAM and the CPU pins (necessary to take advantage of such an improved processor.)

For a traditional CPU to function in harmony, the entire processor must function at a single, synchronized clock speed. This, at least, is the assumption governing traditional microprocessors today. For many years, increasing clock speeds was the industry obsession. When this ceased to be possible and when mobile devices became a larger part of the market share than PCs and laptops, power-saving became the priority. Clock-speed throttling and CPU hibernation became ubiquitous by 2013. Allthwhile, the fundamental assumption that a CPU may operate only at one clock-speed at a given time was never challenged.

## Abstract

Just as cellular telephone equipment may be used to handle thousands of digital signals despite those signals being relayed on frequencies that are nearly identical, such advanced signal processing may plausibly be applied to the field of microprocessing.

In a microprocessor, switches cycle power off and on at a rate of about four billion times per second. This would seem to be extremely difficult for a signal processor to keep up with, but, in reality, lies well-within the realm of possibility. Distinct from cellular communications, microprocessors deal in the flow of electrical current rather than free electromagnetism, which is the more common application for techniques such as Fourier analysis.

Provided that existing MOSFETs are capable of responding to electrical inputs on offset timings, multiple logical processing threads may be routed through the same physical architecture if one is clever in terms of how the signals are routed through such a processor and one has a signal processing architecture capable of identifying, segregating and re-transmitting output data at the end of each processing cycle back to the RAM.

I propose that a novel, improved architecture that shares many features in common with existing architecture may be built upon the central pillar of the unprecedented embedding of signal processors and processor clocks into each pin (or electrical contact, if you prefer) of a CPU. Ordinarily, these pins are merely used as entryways for data into the CPU. In this novel processor type, which may be termed a Shared Architecture Datastream (SAD) Processor, they serve not only as electrical contacts but as modulators of switching frequency in which each pin/signal processor injects instructions/data into the CPU according to a distinct clock speed differing from that associated with the myriad other pins. This is not the only difference between the novel Shared Architecture Datastream CPU and conventional CPUs.

Whereas in a conventional CPU, each pin corresponds to a small portion of the processor and data shunted through that pin is handled only by that one small sub-portion of the overall chip, in the SAD, data entering through any pin is, at some point, handled by the entire processor. In theory, processing power would be improved if inputs from all pins had the benefit of passing through all possible relevant sections of the processor. This architecture would, incidentally, render obsolete multi-core architectures.

In the SAD CPU, the processor is more-fully exploited in this regard, in addition to the obvious benefits of being able to perform 200-300 simultaneous cycles worth of computations, albeit at different timings, on the same architecture and within a single overall cycle.

In the Shared Architecture Datastream chip, each pin's clock may be offset by, for instance, 2 Megahertz. Each of ~250 pins could be offset along the lines of 4.000 GHz, 4.002 GHz, 4.004 GHz, et cetera. Each pin's data (inbound to the CPU,) furthermore, would be handled by the CPU in a manner quite different

from a traditional architecture. To both prevent interference between the multiple overlapping logical processor threads and to ensure the most complete possible use of the computing power of the processor, the SAD CPU would take on a round shape rather than that of a square. The current carrying data throughout the processor would, in a manner of speaking, circulate. It would first move directly toward the interior of that circle down a primary pathway and would then follow an circular path (still featuring the sort of branching bifurcations found in CPUs at the micro-scale) similar to the way data is written to an read from a Compact Disc.

The current would branch outward, following forking (but curved) pathways until it neared the perimeter, at which point, return pathways would ensure that processed data is returned via the same pin through which it entered. The signal processor/clock in a given pin would translate the ~4.000 GHz impulses back into a motherboard-compatible frequency for further use by the system.

## **Conclusion**

As the frequency at which electricity is alternated is varied in this proposed system and the design of the pathways reduce interference by ensuring that signals in-processing “follow” some modest distance behind one another, modern signal processors should be able to retrieve computational results with relative ease.

It may be helpful to investigate whether it is possible to develop transistors featuring semiconductors with a greater degree of ephemerality of capacitance as this may be critical to rendering practical the aforementioned design.